# Bibliography of Papers related to Reversible Logic

last update: May 2013

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## Contents

# 1 Introduction

This document provides a list of reversible logic papers and categorizes them according to the topic they are addressing. There is likely to be overlap, and there is likely to be disagreement on appropriate categorization. However the main purpose of this categorization is to provide some direction for students pursuing any of these topics for research or undergraduate projects, and thus this is intended only to be a starting point.

Updates are welcome and should be emailed to j.rice@uleth.ca with full bibliographic details, the topic(s) under which to list the paper(s) and if possible a pdf of the paper to be added.

# 2 Reversible Logic in General

- 1961: Irreversibility and Heat Generation in the Computing Process [Lan61]
- 1973: Logical Reversibility of Computation [Ben73]
- 1979: Conservative Logic Elements and Their Universality [SK79]
- 1980: Reversible Computing [Tof80]
- 1982: Conservative Logic [FT82]
- 1986: Quantum mechanical computers [Fey86]
- 1991: Optoelectronic, Multivalued, Conservative Logic [Pic91]
- 1994: Results on two-bit gate design for quantum computers [DS94]
- 2003: Time, space, and energy in reversible computing [Fra03]
- 2005: Thermodynamical cost of reversible computing [LT05]
- 2005: Reversible Logic, Pan and Nalasani [PN05]
- 2005: Time, space, and energy in reversible computing [Vit05]
- 2005: Approaching the Physical Limits of Computing [Fra05a]
- 2005: Introduction to Reversible Computing: Motivation, Progress, and Challenges [Fra05b]
- 2009: On the CNOT-cost of TOFFOLI gates, Shende & Markov [SM09]

- 2011: From Truth Tables to Programming Languages: Progress in the Design of Reversible Circuits, Drechsler and Wille [DW11]
- 2012: Reversible Circuits: Recent Accomplishments and Future Challenges for an Emerging Technology, Drechsler and Wille [DW12]
- 2012: Berut, Antoine *et al.*, Experimental verification of Landauer's principle linking information and thermodynamics, [BAP+12]

# 3 Reversible Logic Synthesis

- 2012: Synthesis and Optimization of Reversible Circuits - A Survey, Saeedi and Markov [SM12]
- 2010: Wille and Drechsler, Synthesis of Boolean Functions in Reversible Logic [SB10] (Chapter 4)
- 2011: Wille, R. and Keszöcze, O. and Drechsler, R., Determining the minimal number of lines for large reversible circuits [WKD11]

## 3.1 Group Theory Approaches

- 1999: Group Theoretical Aspects of Reversible Logic Gates [SVJ99]
- 2004: New Classes of Kronecker-Based Reversible Decision Trees and their Group-Theoretic Representations [AR04a]
- 2005: Implementing an Arbitrary Reversible Logic Gate [RVS05]
- 2006: Using Group Theory in Reversible Computing [RVK06]
- 2006: The Decomposition of an Arbitrary Reversible Logic Circuit [VRK06]
- 2007: Synthesis of Reversible Logic for Nanoelectronic Circuits [VR07]
- 2009: Multiple-Valued Reversible Logic Circuits [DR09]

## 3.2 Transformation Approaches

- 2002: Transformation Rules for Designing CNOT-based Quantum Circuits [IKY02]
- 2003: A transformation based algorithm for reversible logic synthesis [MMD03]
- 2003: Transformation-based Synthesis of Networks of Toffoli/Fredkin Gates [DMM03]
- 2005: Synthesis of Fredkin-Toffoli Reversible Networks [MDM05a]
- 2007: Techniques for the synthesis of reversible Toffoli networks [MDM07]
- 2007: A novel synthesis algorithm for reversible circuits, Saeedi, Sedighi and Zamani [SSZ07]
- 2008: Moving forward: A non-search based synthesis method toward efficient CNOT-based quantum circuit synthesis algorithms, Saeedi, Zamani and Sedighi [SZS08]
- 2010: ESOP-Based Toffoli Network Generation with Transformations [SD10]

### 3.3 Templates

- 2003: (this is the paper to cite for work on templates) A Transformation Based Algorithm for Reversible Logic Synthesis, Miller, Maslov and Dueck [MMD03]
- 2003: Fredkin/Toffoli Templates for Reversible Logic Synthesis[MDM03a]
- 2003: Simplification of Toffoli Networks via Templates[MDM03b]
- 2003: Templates for Toffoli Network Synthesis[MDM03c]
- 2005: Toffoli Network Synthesis with Templates[MDM05b]
- 2007: Techniques for the synthesis of reversible Toffoli networks[MDM07]

### 3.4 ESOP-based Approaches (and related)

- 2007: ESOP-based Toffoli Gate Cascade Generation [FTR07] (this is the original ESOP-based synthesis work)
- 2009: Toffoli Gate Cascade Generation Using ESOP Minimization and QMDD-Based Swapping [RFTK09]
- 2009: Generating Toffoli Networks from ESOP Expressions [SD09]
- 2010: ESOP-Based Toffoli Network Generation with Transformations [SD10]
- 2010: Using Autocorrelation Coefficients-based Cost Functions in ESOP-based Toffoli Gate Cascade Generation [RS10]
- 2010: Near-Optimal Ordering of ESOP Cubes for Toffoli Networks [HD10]
- 2010: Decomposition of Reversible Logic Function Based on Cube-Reordering [LKPK11]
- 2010: Rule-Based Optimization of Reversible Circuits, Arabzadeh, Saeedi and Zamani [ASZ10]
- 2011: Ordering Techniques for ESOP-Based Toffoli Cascade Generation [RN11]
- 2011: Improved ESOP-based Synthesis of Reversible Logic [NR11a]

### 3.5 Peres and other (non-Toffoli) Gates

- 2003: Improved quantum cost for n-bit Toffoli gates [MD03c]
- 2008: Reversible logic synthesis with Fredkin and Peres gates [DJ08]

### 3.6 Decision Diagram-Based Approaches

- 2006: Analysis and Synthesis of Quantum Circuits by Using Quantum Decision Diagrams [AP06]
- 2006: QMDD: A Decision Diagram Structure for Reversible and Quantum Circuits [MT06]
- 2006: A Decision Diagram Package for Reversible and Quantum Circuit Simulation [TMG06]
- 2009: Equivalence Checking of Reversible Circuits [WGMD09]
- 2009: BDD-based synthesis of reversible logic for large functions [WD09]
- 2010: BDD-Based Synthesis of Reversible Logic, Robert Wille and Rolf Drechsler [WD10]

### 3.7 Cycle-Based Approaches

- 2009: A cycle-based synthesis algorithm for reversible logic, Sasanian, Saeedi, Sedighi and Zamani [SSSZ09]
- 2010: Reversible circuit synthesis using a cycle-based approach, Saeedi, Zamani, Sedighi and Sasanian [SZSS10]
- 2010: A library-based synthesis methodology for reversible logic, Saeedi, Zamani and Sedighi [SSZ10]

### 3.8 Other Approaches (grouped somewhat by topic)

- 2001: A General Decomposition for Reversible Logic [PJM$^+$01]
- 2001: Regular Realization of Symmetric Functions using Reversible Logic [PKB$^+$01b]
- 2001: Regularity and Symmetry as a Base for Efficient Realization of Reversible Logic Circuits [PKB$^+$01a]
- 2002: Synthesis of Multipurpose Reversible Logic Gates [Ker02]
- 2002: Logic Synthesis of Reversible Wave Cascades [MP02]
- 2002: Reversible Logic Synthesis by Iterative Compositions [KPK02]
- 2003: Multi-Output ESOP Synthesis with Cascades of New Reversible Gate Family [KP03]
- 2004: A New Heuristic Algorithm for Reversible Logic Synthesis [Ker04]
- 2004: Synthesis of Reversible Logic [AJ04]
- 2006: An Algorithm for Synthesis of Reversible Logic Circuits [GAJ06]
- 2002: Spectral and Two-Place Decomposition Techniques in Reversible Logic [Mil02]
- 2007: Techniques for the synthesis of reversible Toffoli networks [MDM07]
- 2004: A Synthesis Method for MVL Reversible Logic [MDM04]
- 2002: Reversible Logic Circuit Synthesis [SPMH02]
- 2003: Synthesis of Reversible Logic Circuits [SPMH03]
- 2003: Garbage in Reversible Designs of Multiple-Output Functions [MD03b]
- 2003: Reversible Function Synthesis with Minimum Garbage Outputs [DM03]
- 2003: Complexity of Reversible Toffoli Cascades and EXOR PLAs [MD03a]
- 2003: Reversible Logic Synthesis (PhD Thesis) [Mas03]
- 2003: Improved quantum cost for n-bit Toffoli gates [MD03c]
- 2004: Reversible Cascades with Minimal Garbage [MD04]
- 2003: Spectral Techniques for Reversible Logic Synthesis [MD03d]

- 1978: Realization of Minimum Circuits with Two-Input Conservative Logic Elements [SK78b]
- 1978: Cascade Realization of 3-Input 3-Output Conservative Logic Circuits [SK78a]

- 2003: Evolutionary approach to Quantum and Reversible Circuits synthesis [LPG+03]
- 2003: Evolutionary Synthesis of Logic Circuits Using Information Theory [AC03]
- 2004: Genetic algorithm based synthesis of multi-output ternary functions using quantum cascade of generalized ternary gates [KP04]
- 2008: Evolutionary approach to quantum symbolic logic synthesis [LP08]
- 2011: Improving ESOP-Based Synthesis of Reversible Logic Using Evolutionary Algorithms, Drechsler, Finder and Wille [DFW11]

- 2008: Bi-Directional Synthesis of 4-Bit Reversible Circuits [YSHP08]

- 2008: Quantum Circuit Simplification and Level Compaction [MDMN08]
- 2010: Reducing the Number of Lines in Reversible Circuits [WSD10]
- 2010: Reducing Reversible Circuit Cost by Adding Lines [MWD10]

- 2007: Fast Exact Toffoli Network Synthesis of Reversible Logic [WG07]
- 2012: Exact Synthesis of Toffoli Gate Circuits with Negative Control Lines, Wille, Soeken, Przigoda and Drechsler [WSPD12]

- 2007: On the Behavior of Substitution-based Reversible Circuit Synthesis Algorithms: Investigation and Improvement Saeedi, Zamani and Sedighi [SZS07]

- 2010: Lowering the Quantum Gate Cost of Reversible Circuits, Miller and Sasanian [MS10]

- 2012: Circuit Line Minimization in the HDL-Based Synthesis of Reversible Logic, Wille, R. and Soeken, M. and Schonborn, E. and Drechsler, R. [WDOGO12]

### 3.9 Post-synthesis Optimization

- 2011: Synthesis of quantum circuits for linear nearest neighbor architectures
  Saeedi, Wille and Drechsler [SWD11]

## 4 Testing and Testability of Reversible Logic Circuits

- 2004: Online Testable Reversible Logic Circuit Design using NAND Blocks [VLP04]
- 2003: Fault testing for reversible circuits, Patel, Hayes and Markov [PHM03]
- 2004: Fault testing for reversible circuits, Patel, Hayes and Markov [PHM04]

- 2004: Testing for Missing-Gate Faults in Reversible Circuits, Hayes, Polian and Becker [HPB04]
- 2005: Synthesis of Reversible Circuits for Testing with Universal Test Set and C-Testability of Reversible Iterative Logic Arrays Chakraborty [Cha05]
- 2005: A Family of Logical Fault Models for Reversible Circuits, Polian, Hayes, Fiehn and Becker [PHFB05]
- 2005: Reversible Fault-Tolerant Logic [BR05]
- 2005: The construction of a fault tolerant reversible gate for quantum computation [VLP05]
- 2005: Test generation and fault localization for quantum circuits [PBL05]
- 2006: Constructing Online Testable Circuits using Reversible Logic, Mahammad, Hari, Shroff and Kamakoti [MHSK06]
- 2006: Reversible-Logic Design With Online Testability [VLDP06]
- 2006: Fault-Tolerant Reversible Circuits [Par06]
- 2006: Analyzing Fault Models for Reversible Logic Circuits [ZM06]
- 2007: Fault tolerant error coding and detection using reversible gates [JSJS07]
- 2007: A DFT methodology for detecting bridging faults in reversible logic circuits, Bubna, M. and Goyal, N. and Sengupta, I. [BGS07]
- 2007: Optimum Test Set for Bridging Fault Detection in Reversible Circuits
  Rahaman, H. and Kole, D.K. and Das, D.K. and Bhattacharya, B.B. [RKDB07]
- 2008: Design of a Novel Fault Tolerant Reversible Full Adder for Nanotechnology Based Systems [HN08]
- 2008: Minimization of CTS of k-CNOT Circuits for SSF and MSF Model, Ibrahim, Chowdhury and Babu [ICB08a]
- 2008: On the Minimization of Complete Test Set of Reversible k-CNOT Circuits for Stuck-at Fault Model,Ibrahim, Chowdhury and Babu [ICB08b]
- 2008: On the Detection of Missing-Gate Faults in Reversible Circuits by a Universal Test Set, Rahaman, Kole, Das and Bhattacharya [RKDB08]
- 2008: Fault detection for single and multiple missing-gate faults in reversible circuits, Xiao Fang-ying and Chen Han-wu and Liu Wen-jie and Li Zhi-giang [FyHwWjZg08]
- 2008: Universal test set for bridging fault detection in reversible circuit, Sarkar, P. and Chakrabarti, S. [SC08]
- 2009: Synthesis of Fault Tolerant Reversible Logic Circuits[IRB+09]
- 2009: Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders[IRBH09]
- 2010: Fault Models for Quantum Mechanical Switching Networks, Biamonte, Allen and Perkowski [BAP10]
- 2010: Constructing Online Testable Circuits Using Reversible Logic, Mahammad and Veezhinathan [MV10]
- 2010:Synthesis of online testable reversible circuit, Kole, D.K. and Rahaman, H. and Das, D.K. and Bhattacharya, B.B. [KRDB10b]
- 2010: Derivation of Optimal Test Set for Detection of Multiple Missing-Gate Faults in Reversible Circuits, Kole, D.K. and Rahaman, H. and Das, D.K. and Bhattacharya, B.B. [KRDB10a]
- 2010: Online Multiple Fault Detection in Reversible Circuits, Farazmand, N. and Zamani, M. and Tahoori, M.B. [FZT10a]
- 2010: Online fault testing of reversible logic using dual rail coding, Farazmand, N. and Zamani, M. and Tahoori, M.B. [FZT10b]

- 2011: Online Testable Ternary Reversible Circuit, Rahman and Rice [RR11a]
- 2011: On Designing a Ternary Reversible Circuit for Online Testability, Rahman and Rice [RR11b]
- 2011: Online Fault Detection in Reversible Logic, Nayeem and Rice [NR11b]
- 2011: A Simple Approach for Designing Online Testable Reversible Circuits, Nayeem and Rice [NR11c]
- 2011: Derivation of Automatic Test Set for Detection of Missing Gate Faults in Reversible Circuits, Kole, D.K. and Rahaman, H. and Das, D.K. and Bhattacharya, B.B [KRDB11]
- 2011: Online Missing/Repeated Gate Faults Detection in Reversible Circuits Zamani, M. and Tahoori, M.B., [ZT11]
- 2011: Fault Masking and Diagnosis in Reversible Circuits, Zamani, M. and Farazmand, N. and Tahoori, M.B. [ZFT11]
- 2011: Debugging reversible circuits, Robert Wille, Daniel Große, Stefan Frehse, Gerhard W. Dueck and Rolf Drechsler [WGF+11]
- 2012: Design of an Online Testable Ternary Circuit from the Truth Table, Nayeem and Rice [NR12]
- 2012: A DFT methodology targeting online testing of reversible circuit, Sen, B. and Das, J. and Sikdar, B.K. [SDS12]

# 5 Fault Tolerant Reversible Logic/Computing

- 2005: The construction of a fault tolerant reversible gate for quantum computation, Vasudevan *et al.* [VLP05]
- 2005: Reversible fault-tolerant logic, Boykin and Roychowdhury [BR05]
- 2006: Fault-Tolerant Reversible Circuits, Parhami [Par06]
- 2009: Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders, Islam, Rahman, Begumand and Hafiz [IRBH09]
- 2009: Synthesis of Fault Tolerant Reversible Logic Circuits, Islam, Rahman, Begum, Hafiz and Al Mahmud [IRB+09]
- 2012: Minimum Cost Fault Tolerant Adder Circuits in Reversible Logic Synthesis, Mitra and Chowdhury [MC12]

# 6 Connections to Quantum Computing

- 1995: Quantum Computation [DiV95]
- 2000: The Physical Implementation of Quantum Computation [DiV00]
- 2000: Quantum Computation and Quantum Information [NC00]
- 2000: Multivalued logic gates for quantum computation, Muthukrishnan and Stroud [MS00]
- 2002: Multiple-Valued Quantum Logic [ARCP02]
- 2003: Improving Gate-Level Simulation of Quantum Circuits [VMH03]
- 2004: Quantum Circuit Synthesis Using Classes of GF(3) Reversible Fast Spectral Transforms [AR04b]
- 2005: Graph-based Simulation of Quantum Computation in the Density Matrix Representation [VMH05a]

- 2005: Is Quantum Search Practical? [VMH05b]
- 2006: A Decision Diagram Package for Reversible and Quantum Circuit Simulation [TMG06]
- 2006: Analysis and Synthesis of Quantum Circuits by Using Quantum Decision Diagrams [AP06]
- 2006: QMDD: A Decision Diagram Structure for Reversible and Quantum Circuits [MT06]
- 2006: Quantum Programming Languages Survey and Bibliography, Gay [Gay06]
- 2007: Quantum Logic Circuit Simulation Based on the QMDD Data Structure [GTFM07]
- 2008: Quantum Circuit Simplification and Level Compaction [MDMN08]
- 2009: Toffoli Gate Cascade Generation Using ESOP Minimization and QMDD-Based Swapping [RFTK09]
- 2011: Reversible Circuit Optimization Via Leaving the Boolean Domain, Maslov and Saeedi [MS11]
- 2012: Constant-optimized quantum circuits for modular multiplication and exponentiation, Markov and Saeedi [MS12]
- 2012: Synthesis of reversible circuits with minimal lines for large functions, Soeken, Wille, Hilken, Przigoda and Drechsler [SWH$^+$12]
- 2013: Faster quantum number factoring via circuit synthesis, Markov and Saeedi [MS13]

# 7 Multiple-Valued Reversible Logic

- 1991: Optoelectronic, Multivalued, Conservative Logic[Pic91]
- 1996: Multi-Valued Sequential Logic Design using Fredkin Gates[Pic96]
- 2000: Multivalued logic gates for quantum computation, Muthukrishnan and Stroud [MS00]
- 2002: Multiple-Valued Quantum Logic[ARCP02]
- 2004: A Synthesis Method for MVL Reversible Logic[MDM04]
- 2004: Genetic algorithm based synthesis of multi-output ternary functions using quantum cascade of generalized ternary gates[KP04]
- 2006: Using Multiple-Valued Gates to Implement Reversible Logic[MBLO06]
- 2006: On Universality of General Reversible Multiple-Valued Logic Gates[**?**] ADD TO BIB
- 2006: Synthesis of Quantum Multiple-Valued Circuits[MT06]
- 2009: Multiple-Valued Reversible Logic Circuits[DR09]
- 2009: Quantum Realization of Multiple-Valued Feynman and Toffoli Gates Without Ancilla Input, Khan [Kha09]
- 2012: Design of an Online Testable Ternary Circuit from the Truth Table, Nayeem and Rice [NR12]

# 8 Sequential Reversible Logic

- 1996: Multi-Valued Sequential Logic Design using Fredkin Gates[Pic96]
- 2005: A Beginning in the Reversible Logic Synthesis of Sequential Circuits[TSZ05]
- 2005: An Extension to DNA Based Fredkin Gate Circuits: Design of Reversible Sequential Circuits using Fredkin Gates[TS05a]
- 2006: A New Look at Reversible Memory Elements[Ric06]
- 2006: Reversible Logic Designs for Sequential Elements[CW06]
- 2007: An Introduction to Reversible Latches[Ric07]
- 2008: Synthesis of reversible sequential elements[CW08]
- 2010: Design of reversible sequential circuits optimizing quantum cost, delay, and garbage outputs[TR10]
- 2011: Synthesis of Reversible Synchronous Counters[KP11]
- 2012: A Synthesis Flow for Sequential Reversible Circuits, Soeken, M. and Wille, R. and Otterstedt, C. and Drechsler, R. [SWOD12]

# 9 Technologies and (Gate) Implementations

- 1994: Reversible logic issues in adiabatic CMOS [AS94]
- 1995: Elementary Gates for Quantum Computations [BBC$^+$95]
- 1995: Asymptotically Zero Power in Reversible Sequential Machines [Pat95]
- 1996: Energy Recovery Circuits Using Reversible and Partially Reversible Logic [YR96]
- 2000: The Physical Implementation of Quantum Computation [DiV00]
- 2000: A three-port nRERL register file for ultra-low-energy applications [KLC00]
- 2002: NAND/NOR Adiabatic Gates: Power Consumption Evaluation and Comparison Versus the Fan-In, Alioto and Palumbo [AP02]
- 2002: Desoete, Bart and De Vos, Alexis, A reversible carry-look-ahead adder using control gates [DDV02]
- 2005: Making Adiabatic Circuits Attractive for Todays VLSI Industry by Multi-mode Operation-adiabatic Mode Circuits [HNE$^+$05]
- 2005: Reversible Computing: From Mathematical Group Theory to Electronical Circuit Experiment [VR05]
- 2005: Implementation of a Simple 8-bit Microprocessor with Reversible Energy Recovery Logic [KC05]
- 2006: Using Multiple-Valued Gates to Implement Reversible Logic [MBLO06]
- 2008: J. Chen *et al.*, Extended Toffoli gate implementation with photons [CZW$^+$08]
- 2012: De Vos, Alexis and Burignat, Sté phane and Thomsen, Michael Kirkedal, Reversible implementation of a discrete integer linear transformation [DVBT12]
- 2012: Wille, R. and Drechsler, R. and Osewold, C. and Garcia-Ortiz, A., Automatic design of low-power encoders using reversible circuit synthesis [WDOGO12]

## 10 Circuits and Designs

- 2005: A Novel Reversible TSG Gate and Its Application for Designing Reversible Carry Look-Ahead and Other Adder Architectures, Thapliyal and Srinivas [TS05a]
- 2005: A Novel Reversible TSG Gate and Its Application for Designing Reversible Carry Look Ahead Adder and Other Adder Architectures, Thapliyal and Srinivas [TS05b]
- 2005: The construction of a fault tolerant reversible gate for quantum computation, Vasudevan *et al.* [VLP05]
- 2006: A new approach to synthesize multiple-output functions using reversible programmable logic array[CNB06]
- 2006: Novel BCD Adders and their Reversible Logic Implementation for IEEE 754r Format, Thapliyal, Kotiyal and Srinivas [TKS06]
- 2008: Efficient approaches for designing reversible Binary Coded Decimal adders[BHCB08]
- 2008: Design of a Novel Fault Tolerant Reversible Full Adder for Nanotechnology Based Systems[HN08]
- 2009: Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders[IRBH09]
- 2010: Adder Designs using Reversible Logic Gates, Lala, Parkerson and Chakraborty [LPC10]
- 2011: Synthesis of Reversible Synchronous Counters[KP11]
- 2012: An efficient approach for designing and minimizing reversible programmable logic arrays[MJKHB12]
- 2013: Design of a 4-bit 2's Complement Reversible Circuit for Arithmetic Logic Unit Applications, [SSMT13]

## 11 Resources

- 2008: RevLib: An Online Resource for Reversible Functions and Reversible Circuits[WGT$^+$08]
- 2008: Reversible Logic Synthesis Benchmarks Page[MDS08]

## 12 Books

- 2004: Reversible Logic Synthesis [AR04b]

## 13 Related Resources

- 1999: Sasao, Switching Theory for Logic Synthesis [Sas99]
- 2002: International Technology Roadmap for Semiconductors (ITRS) [ITR02]; 2009 update [ITR09]; 2011 update [ITR11]
- 2008: Multiple Valued Logic: Concepts and Representations[MT08]

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[AS94] W. C. Athas and L. J. Svensson. Reversible logic issues in adiabatic CMOS. In *Proceedings of the Workshop on Physics and Computation (PhysComp)*, pages 111–118, Dallas, TX, 1994.

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[BAP10] Jacob D. Biamonte, Jeff S. Allen, and Marek A. Perkowski. Fault models for quantum mechanical switching networks. *(JETTA)*, 26(5):499–511, 2010.

[BAP+12] Antoine Berut, Artak Arakelyan, Artyom Petrosyan, Sergio Ciliberto, Raoul Dillenschneider, and Eric Lutz. Experimental verification of landauer's principle linking information and thermodynamics. *Nature*, 483:187–189, 2012.

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[BGS07] M. Bubna, N. Goyal, and I. Sengupta. A DFT methodology for detecting bridging faults in reversible logic circuits. In *Proceedings of TENCON – IEEE Region 10 Conference*, pages 1–4, 30 2007-nov. 2 2007.

[BHCB08] Ashis Kumer Biswas, Md. Mahmudul Hasan, Ahsan Raja Chowdhury, and Hafiz Md. Hasan Babu. Efficient approaches for designing reversible Binary Coded Decimal adders. *Microelectronics Journal*, 39(12):1693–1703, 2008.

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[Cha05] A. Chakraborty. Synthesis of reversible circuits for testing with universal test set and C-testability of reversible iterative logic arrays. In *Proceedings of the 18th International Conference on VLSI Design*, pages 249–254, 2005.

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[CZW+08] J. Chen, X. Zhang, L. Wang, X. Wei, and W. Zhao. Extended Toffoli gate implementation with photons. In *Proceedings of 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT)*, pages 575–578, China, 20-23 Oct 2008.

[DDV02] Bart Desoete and Alexis De Vos. A reversible carry-look-ahead adder using control gates. *Integr. VLSI J.*, 33(1):89–104, December 2002.

[DFW11] Rolf Drechsler, Alexander Finder, and Robert Wille. Improving ESOP-based synthesis of reversible logic using evolutionary algorithms. *EvoApplications*, 2:151–161, 2011.

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[DiV00] David P. DiVincenzo. The physical implementation of quantum computation. *Fortschritte der Physik*, 48(9–11):771–783, Sept. 2000.

[DJ08] James Donald and Niraj K. Jha. Reversible logic synthesis with Fredkin and Peres gates. *Journal of Emerging Technologies in Computer Systems*, 4(1):2:1–2:19, April 2008.

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[DMM03] G. W. Dueck, D. Maslov, and D. M. Miller. Transformation-based synthesis of networks of Toffoli/Fredkin gates. In *Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering*, pages 211–214, vol.1, 2003.

[DR09] A. De Vos and Y. Van Rentergem. Multiple-valued reversible logic circuits. *Journal of Multiple-Valued Logic & Soft Computing*, 15(5/6):489–505, 2009.

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